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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/726,144	WORRELL, FRANK	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,4,5,14 and 16* is/are allowed.

6)☒ Claim(s) *2,3,6-13 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 and 16-20 have been examined.

Papers Received

2. Receipt is acknowledged of the amendment papers, where the paper has been placed of record in the file.

3. The 35 USC 112 rejections have been overcome by the amendment and are herein withdrawn. However, new 35 USC 112 issues have been found as set forth below.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 7-13 and 17-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 7 states that a branch target address, a sequential instruction address immediately following the branch instruction address, and a recovery address immediately following the sequential address are all provided to a multiplexer in a single pipeline cycle. The specification does not give an adequate description of how all three of the addresses are presented in the same cycle to the multiplexer nor would it enable one of ordinary skill in the art to make or use the invention without undue

experimentation. Figures 1 and 2 as well as pages 6-9 of the specification give description and illustration of a pipeline **stage** where a multiplexer receives all of the addresses at some point but nowhere is it mentioned that all three are provided in the same cycle within this stage. In fact, one of ordinary skill in the art would expect that a recovery address, which is immediately following the sequential address, would be received by the multiplexer a cycle after the sequential address is received. The only time this would not be necessarily expected is if the invention was disclosed as fetching multiple instructions per cycle and thus all three addresses would be needed in order to select the correct instruction to fetch. However, multiple places in the specification including page 4 for example show such language as "a program counter address of *an instruction* being fetched", which clearly illustrates that only a single instruction is fetched each cycle. Further, the presented arguments do not clarify this matter. With this being the case, one of ordinary skill in the art would not recognize how to make or use a single multiplexer receiving an address of an instruction and the address of the instruction after it in a single pipeline cycle without undue experimentation.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Trauben (5,509,130).

8. In regard to claim 2, Trauben discloses a method of conditional branching in a pipelined processor (figure 9 gives the flow of the pipeline stages), the method comprising the steps of:

a. fetching a first instruction stored at a branch target address in response to encountering a branch instruction, at a program counter address; [Figure 10a shows that when a branch instruction (BNE) is encountered or decoded (d0 and d1), the first Target is fetched (T1). Figure 1, element 12 shows that a program counter exists in the system. Column 5, lines 35-46 show that the program counter is used for issuing instructions and its function does not need to be described because it is well know in he art. This well known in the art function is that the program counter points to the addresses of instructions that are fetched for execution.]

b. decoding a second instruction stored at a next address immediately following said program counter address during a same pipeline cycle as said fetching; [Figure 10a shows that a delay instruction and the sequential instruction after it are decoded while fetching T1. Column 18, lines 51-60 further explain that these are sequential instructions with respect to the branch (because of their placement in the sequential queue) that decode while the target is fetched. As shown in column 18, line 44 – column 19, line 40 along with figure 10, instructions are fetched and sent through the pipeline in pairs and thus have a

single fetch address for the pair. Therefore, the sequential and delay instruction pair shown in figure 10a as group 164 was fetched at an address immediately following the program counter address of the branch since this is the next address pointed to by the program counter.]

c. evaluating between taking a branch defined by said branch instruction and not taking said branch during said same pipeline cycle as said fetching. [Column 18, line 61 shows that at time 6, the branch is resolved, meaning that it was being evaluated during time 5, or while the fetching was occurring. Figure 10a further shows with arrows that the execute stage e0 determines the condition of the branch so the next instructions to be decoded are known and that this evaluation occurs at the same time as the fetching of the target T1.]

d. And fetching a third instruction stored at a sequential instruction address immediately following said branch target address in response to determining to take said branch. [Figure 10a shows the case where the branch is taken (column 18, lines 40-41). The figure also shows (along with the cited text) that the next sequential target instruction group 168 (one of which we will call the third instruction) is fetched in response to the evaluation of the branch in stage e0. As shown above, since the instructions are fetched in pairs, the immediately following address after the target instructions' (group 166) address is that of group 168.]

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Trauben in view of Hennessy.

11. In regard to claim 3,

a. Trauben discloses the method of claim 2;

b. Trauben does not explicitly disclose further comprising the step of: generating said sequential instruction address based upon said program counter address and a predetermined offset.

c. However, Trauben has shown in column 5, lines 35 – 46 that a program counter is used and the program counter is intended to be among a broad category of program counters found in most pipelined processors. Hennessy has disclosed on pages 385 and 404 the use of a program counter that is incremented by a predetermined offset to generate the next sequential instruction address.

d. Since Trauben has taught that any program counter may be used one of ordinary skill in the art would have been motivated to modify the design of Trauben to use the program counter and update method taught by Hennessy.

> Trauben has taught that the system of use involves fixed length instructions (column 2, lines 54-62) and thus the program counter incrementation method would work successfully to address the sequential instruction address, which may be the address of a group of two sequential instructions (figure 10).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Trauben to us the program counter and method for updating taught by Hennessy since Trauben discloses that any program counter among a broad category of common program counters may be used.

12. In regard to claim 6, similar language is used (in part) to that of claim 2 concerning the fetching of an instruction in response to determining not to take said branch and thus the same arguments provided above for claim 2 apply to this portion of claim 6. In addition, the use of updating a program counter and an exception program counter is disclosed above for claim 3 and thus the same arguments apply here. Concerning the limitation regarding generating the branch target address based on a displacement, Trauben shows in column 18, lines 16-19 that the branch target address is computed. Trauben also discloses the existence of a program counter as shown above. Since the target address must be computed, an absolute address cannot be taken. Thus it is inherent that the branch address is computed using the current address (program counter) and some displacement pointing to the next instruction.

Response to Arguments

13. Applicant's arguments filed 26 May 2004 in regards to claims 2, 3, and 6 have been fully considered but they are not persuasive.

14. In regard to claim 2, Applicant argues that figure 10a of Trauben appears to show that a Target 2 instruction immediately following a Target 1 instruction is fetched at the same time as the Target 1 instruction before a determination to take a branch is made. Figure 10a shows the case where the branch is taken (column 18, lines 40-41). The figure also shows (along with the cited text) that the next sequential target instruction group 168 (one of which we will call the third instruction) is fetched in response to the evaluation of the branch in stage e0. As shown in column 18, line 44 – column 19, line 40 along with figure 10, instructions are fetched and sent through the pipeline in pairs and thus have a single fetch address for the pair. Since the instructions are fetched in pairs, the immediately following address after the target instructions' (group 166) address is that of group 168.

15. No specific arguments on the individual limitations other than those inherited from the parent claim 2 have been entered for claims 3 and 6.

16. The arguments for claims 7-13 and 17-20 are not necessarily persuasive, however, the art rejections of these claims has been withdrawn due to the enablement problem given above. Because one of ordinary skill in the art would not have seen how to make or use the invention without undue experimentation no art has been currently found to disclose the subject matter of such a claim.

Allowable Subject Matter

17. Claims 1, 4, 5, 14, and 16 are allowed.

Conclusion

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

19. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-4166. The examiner can normally be reached on M-F 6:30-4:00 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
February 22, 2005

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